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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/659,256	09/11/2000	Alan S. Krech JR.	10001846-1	5584

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EXAMINER

SHRADER, LAWRENCE J

ART UNIT	PAPER NUMBER
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2124

DATE MAILED: 08/01/2003

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)
	09/659,256	KRECH ET AL.
Examiner	Art Unit	
Lawrence Shrader	2124	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 03 June 2003 .

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 12 - 14 is/are allowed.

6) Claim(s) 1 - 11, and 15 - 18 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____ .

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____ .

2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ . 6) Other: _____ .

DETAILED ACTION

1. This action is in response to the reconsideration filed on June 3, 2002.
2. Claims 1 – 11, and 15 - 18 remain rejected under 35 USC § 103 and repeated below.
3. Claims 12 – 14 are allowed.

Specification

4. The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Rejection of claims 1 – 11, and 15 - 18 is maintained and repeated below.

6. Claims 1, 4 - 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans).

In reference to claim 1, Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67). Kamiyama does not teach a first selector and a second flag selector. Vidwans teaches a set of multiplexers that select a first set of signals (flags), which in turn feed a second selector creating a single flag bit as output (Figure 6). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the sequencer and branching unit as taught by Kamiyama and Vidwans in order to provide a multiple stage input selector that would produce a single branching bit as a condition for a branch to be executed.

In reference to claims 4 – 5, the rejection of claim 1 is incorporated with Vidwans disclosing the use of a two stage multiplexer (Figure 9).

7. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) as applied to claim 1,

and further in view of Asakawa et al., U.S. Patent 5,408,620 (hereinafter referred to as Asakawa).

Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67), but neither Kamiyama nor Vidwans teach a plurality of branch instruction units comprising an operator logically combining branch flags to create a branch bit. Asakawa, however, teaches multiple branch instruction units (column 2, lines 50 – 56), and a circuit for processing conditional branching instructions that uses a multiple input logical AND as an operator (column 5, line 49 to column 6, line 54; Figure 7, item 132). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to further modify the combination of Kamiyama and Vidwans with the teaching of Asakawa to operate multiple branching units, and to provide an operator accepting multiple flags and logically combining in order to produce a branching bit indicating a certain condition to enhance the combination of Kamiyama and Vidwans.

In reference to claim 6, the rejection of claim 2 in incorporated and references the multiple input logical AND operator (Asakawa: Figure 7, item 132).

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) as applied to claim 1, and further in view of Runaldue et al., U.S. Patent 5,479,649 (hereinafter referred to as Runaldue).

Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67), but neither Kamiyama nor Vidwans teaches the use of programmable registers. Runaldue teaches the use of programmable registers (column 5, lines 46 – 54). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the sequencer and branching unit as taught by Kamiyama and Vidwans with programmable registers as taught by Runaldue in order to store the condition flags and supply them to the logic circuits in determination of a branch condition.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) as applied to claim 1, and further in view of Ochiai et al., U.S. Patent 4,742,466 (hereinafter referred to as Ochiai).

Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (column 1, lines 25 – 30), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67), but neither Kamiyama nor Vidwans teaches the use of a branch address comprising a plurality of bits in a conditional branch instruction. Ochiai teaches the use of a branch address comprising a plurality of bits in a conditional branch instruction (column 3, lines 1 – 4). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the sequencer and branching unit as taught by

Kamiyama and Vidwans with a branch address as a plurality of bits in a conditional branch instruction as taught by Ochiai in order to provide the branch address in the case of a branch.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) as applied to claim 1, and further in view of Webb et al., U.S. Patent 6,067,617 (hereinafter referred to as Webb).

The rejection of claim 1 is incorporated, and Webb further teaches the use of a conditional branch instruction comprising a bit that allows branching on various combinations of flag settings (column 9, lines 20 – 26). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the sequencer and branching unit as taught by Kamiyama and Vidwans with a conditional branch instruction bit as taught by Webb in order determine on which condition to branch.

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) and further in view of Asakawa et al., U.S. Patent 5,408,620 (hereinafter referred to as Asakawa) and of Webb et al., U.S. Patent 6,067,617 (hereinafter referred to as Webb).

The rejection of claim 2 is incorporated. Claim 9 is rejected for the same reason put forth in the rejection of claim 8.

In reference to claims 10 and 11, official notice is taken that a dual input, single output selector/multiplexer is well known in the art with inputs arranged in various configurations.

12. Claims 15 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) and further in view of Ochiai et al., U.S. Patnet 4,742,466 (hereinafter referred to as Ochiai).

In reference to claim 15, Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67). Kamiyama does not teach a first selector and a second flag selector. Vidwans teaches a set of multiplexers that select a first set of signals (flags), which in turn feed a second selector creating a single flag bit as output (Figure 9). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the sequencer and branching unit as taught by Kamiyama and Vidwans in order to provide a multiple stage input selector that would produce a single branching bit as a condition for a branch to be executed.

Neither Kamiyama nor Vidwans teaches a compiler, but Ochiai teaches a compiler that converts source code including conditional branch instructions including an address and a flag (column 2, line63 to column 3, line 12). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the compiler as taught by Ochiai with the

sequencer and branching unit as taught by Kamiyama and Vidwans in order to create the object code that is processed in the system.

In reference to claim 16, the rejection of claim 15 is incorporated. Claim 16 is rejected is rejected for the same reason put forth in the rejection of claim 14.

13. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) and of Ochiai et al., U.S. Patnet 4,742,466 (hereinafter referred to as Ochiai) as applied to claim 15, and further in view of Prasanna, U.S. Patent 6,272,599.

Kamiyama, Vidwans, and Ochiai combine to teach a compile to process conditional branch instructions, a sequence of instructions executed as object code, and a branch unit to determine whether to take a branch or not. None teach the compiler setting bits on a certain condition. Prasanna teaches a compiler capable of selectively setting bits based on a certain condition. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine Kamiyama, Vidwans, and Ochiai so that the executable code might be executed by the sequencer and branching unit with equivalent conjunctive logic (incorporated from claim 16) based on a signal flag as further taught by Prasanna.

14. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama) in view of Vidwans et al., U.S. Patent 5,740,393 (hereinafter referred to as Vidwans) and of Ochiai et al., U.S. Patnet 4,742,466

(hereinafter referred to as Ochiai) as applied to claim 15, and further in view of Akiyama, U.S. Patent 5,534,799.

Kamiyama, Vidwans, and Ochiai combine to teach a compile to process conditional branch instructions, a sequence of instructions executed as object code, and a branch unit to determine whether to take a branch or not. None teach arithmetic logic units (ALU) that supply a plurality of flags. Akiyama teaches an ALU that supplies a plurality of flags. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use the teaching of Akiyama to further modify the combination of Kamiyama, Vidwans, and Ochiai so that the executable code might be executed by the sequencer and branching unit supplying flags appropriate to certain conditions required by the branch instruction.

Allowable Subject Matter

15. Claims 12 – 14 are allowed.

Claim 12 is allowed in view of the cited prior art, taken alone or in combination fail to teach "...identifying a flag selection register value for each flag in said set of flags, and storing each said flag selection register value in a respective one of a plurality of flag selection register array elements, assigning a branch condition address for said conditional branching instruction..." Therefore, the rejection of claim 12 is withdrawn. Claims 13 and 14 depending from claim 12 are also allowed.

Response to Arguments

16. Applicant's arguments filed on June 3, 2003 have been fully considered, but they are not persuasive:

(A) Applicant's argument for claim 1:

"Claim 1 is rejected as rendered obvious by US Pat. No. 5,991,868 to Kamiyama (herein "the Kamlyama patent") in view of US Pat. No. 5,740,393 to Vidwans (herein "the Vidwans patent"). Specifically, the Office Action suggests that the Kamiyama patent teaches conditional branching with a flag used to determine if a branch is to occur and the Vidwans patent (Figure 9) teaches first and second sets of multiplexors to create a single flag bit as an output. With all due respects, Applicant believes that Figure 9 of the Vidwans patent and accompanying disclosure teaches an instruction pointer logic circuit that results in a multiple bit value that is transferred to an instruction pointer register over an instruction pointer bus. See column 16, lines 35-37. The terms used in the teachings such as "register" and "bus" imply a multiple bit word although Figure 9 shows a single line as is common for simplified illustrations of bus lines. The purpose of the instruction pointer logic circuit as taught in the Vidwans patent is to determine instruction pointer limit violations and not to process conditional branching as claimed. See column 12, lines 60-65. Claim 1 recites in part "a plurality of first flag selectors, each first flag selector presenting a flag from a plurality of available flags". The Vidwans patent does not suggest or motivate one of ordinary skill in the art to adapt the teachings of the Kamiyama patent to process multiple available flags to arrive at a branch flag that indicates whether to branch according to the conditional instruction as claimed. The combination of the two references cited, therefore, does not include sufficient teachings to arrive at the claimed invention and withdrawal of the rejection is respectfully requested."

Examiner's response:

The teaching of Vidwan, including Figure 9, shows a two stage multiplexer, which reads on the limitation "...a plurality of first flag selectors, each first flag selector presenting a flag from a plurality of available flags...a second flag selector accepting a plurality of said flags and selecting one of said flags to present as a branch flag..." This limitation describes a two-stage

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multiplexer, which Vidwans also discloses. The multiplexing principle illustrated in the Vidwans reference is well known in the art, i.e., whether it multiplexes x n-bit input paths to 1 n-bit output path, or multiplexes x bits to 1 bit output. Therefore, modifying the number and type of inputs would have been well known to one skilled in the art at the time the invention was made in order to produce a branch flag in the Kamiyama invention using the Vidwans two-stage multiplexer in the judging unit.

(B) Applicant's argument for claims 4 and 5:

``With specific reference to claims 4 and 5, Applicant is unable to locate specific rejections in the Office Action. Accordingly, other than the response with respect to claim 1, Applicant is unable to directly address the USPTO position for rejection of these claims. Because claim 1 is believed to be patentable and because claims 4 and 5 depend from claim 1, withdrawal of the rejection of claims 4 and 5 is respectfully requested.''

Examiner's response:

Claims 4 and 5 are referenced at the bottom of page 2 of the first Office Action, and in the same location on page 3 of this action. These claims further indicate the use of a two-stage multiplexer configuration in claim 1, which Vidwans illustrates and is described above.

(C) Applicant's argument for claim 15:

“Claim 15 is rendered obvious by the combination of the Kamiyama, Vidwans and Ochiai patents. In order to render the claim obvious, the combination of the three patents must suggest the claim as a whole to one of ordinary skill in the art. The combination of the Kamiyama, Vidwans, and the Ochiai patents do not sufficiently teach the collective elements of “a branch unit comprising a programmable flag selection memory, a plurality of first flag selectors...a second flag selector accepting a

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plurality of said flags and selecting one of said flags to present as a branch flag". The Kamiyama patent teaches storage of a program status word for storing flag groups to be changed in accordance with the calculation results. See column 4, lines 7-10 of the Kamiyama patent. There is no such flag group storage and changing in the present claim. Claim 15 recites "a programmable flag selection memory". Accordingly, it is a value that selects the appropriate flags that is stored and not the flags themselves. The Vidwans patent in Figure 9 teaches an instruction pointer logic circuit 100. The Vidwans patent does not teach flag processing for purposes of conditional branching. Applicant does not dispute that multiplexors are known. Applicant's position is that the use of the selectors relative to the flags and access to the flags for purposes of processing a conditional branch is nor taught or suggested in the cited art. No where in the Vidwans patent is there a suggestion that would cause one of ordinary skill in the art to combine the teachings of the Kamiyama patent and the Ochiai patents to address flag processing in a context of conditional branching without execution latency to arrive at claim 15 as a whole. The Ochiai patent merely suggests that a branch address may be part of a branch instruction. These three disclosures are insufficient to arrive at the combination as claimed. Accordingly, claim 15 is believed to be patentable over the cited references and withdrawal of the rejection is respectfully requested. ''

Examiner's response:

The reasoning for combining the Kamiyama invention using the Vidwans two-stage multiplexer in the judging unit was given above for claim 1.

17. Arguments for claims 1 – 11, and 15 – 18 have been considered and were not persuasive.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence Shrader whose telephone number is (703) 305-8046. The examiner can normally be reached on M-F 08:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Lawrence Shrader
Examiner
Art Unit 2124

July 30, 2003



Todd Ingberg
Primary Examiner
Group 2100